UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,716	10/28/2003	Toshiyasu Morita	16869D-059900US	6473

20350 7590 08/10/2006

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,716	MORITA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-55,63 and 64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-55,63 and 64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/28/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 31-55, and 63-64 in the reply filed on 4 May 2006 is acknowledged.

Information Disclosure Statement

2. The information disclosure statement filed on 28 October 2003 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the application number of the application for which the information disclosure statement is being submitted is not present on the form (see 37 CFR § 1.98(a)(1)(i)). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Drawings

3. The drawings were received on 28 October 2003. These drawings are deemed acceptable for examination.

Specification

4. The disclosure is objected to because of the following informalities:

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The brief description of the drawings is objected to for failing comply with MPEP § 608.01(f). More specifically, several figures are divided into sub-groupings (i.e. Figure 3, 3A, 3B), however the brief description does not explicitly refer to each of these sub-grouped figures. The brief description should refer to each figure as a whole (i.e. Fig. 3), or each figure individually (i.e. Fig. 3, Fig. 3A, Fig. 3B).

The brief summary of the invention is objected to for failing comply with MPEP § 608.01(d). More specifically, the brief summary should summarize the *claimed* invention (emphasis added), not the disclosure as a whole. Applicant has cancelled several claims in response to a restriction requirement, therefore Examiner respectively requests Applicant modify the brief summary to exclude any and all non-elected (and subsequently cancelled) subject matter.

Appropriate correction is required.

Claim Objections

5. Claim 56 objected to because of the following informalities:

The phrase "the destination address" should be changed to "a destination address" (line 9 of the claim) to properly establish antecedent basis for the phrase.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 56, and 63-64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 56 recites the limitation "the area in the non-volatile memory" in lines 18-19 of the claim. There is insufficient antecedent basis for this limitation in the claim. More specifically, an area of the *dynamic* memory is set forth previously in the claim, however an area of the *non-volatile* memory is not. Which area of the non-volatile memory is being claimed here? Is the entire non-volatile memory being claimed, or just one particular area of said memory?

As for claim 63, the phrase "partial write" as recited on lines 8 and 15 of this claims renders the claim indefinite. More specifically, one of ordinary skill in the art would be unable to ascertain the metes and bounds of this claim limitation, as it is unclear how exactly a partial write of each datum contrasts with a full write of each

datum. Furthermore, the specification provides no guidance as to sufficiently describe exactly what constitutes a "partial write operation".

Claim 64 is rejected for further limiting claim 63.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 31-37, 40-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasbun et al. (US Patent 5,696,929), hereinafter Hasbun.

As for claim 31, Hasbun teaches a memory access method in a data processing unit comprising re-programmable non-volatile memory, the method comprising (Fig. 2, both the cache and holding buffers (23, 25) are composed of DRAM, and the flash memory array (27) is composed of flash EEPROM – col. 3, lines 55-65 and col. 5, lines 11-29):

detecting a write operation to an area in the re-programmable non-volatile memory (Fig. 4, the flow chart begins by attempting a write operation to the main memory (EEPROM));

determining a caching location which identifies an area of memory in a dynamic memory to which data to be written by the write operation can be cached, the area of memory identified by the caching location referred to as a

caching area (Fig. 4, before the data is written to EEPROM (last step of the flow), the system attempts to determine a location to store the data in the cache); and

writing the data to the caching area instead of writing the data to the area in the re-programmable non-volatile memory, wherein the caching area is associated with the area in the re-programmable non-volatile memory (continuing with the flow diagram in Fig. 4, data is written to the cache either by writing it to the appropriate addressed line, or it is written to an empty line).

As for claim 44, Hasbun teaches a data processing unit comprising:

a bus for accessing a dynamic memory (Fig. 1, memory bus – see also in Fig. 2, the flash controller serves as an interface between the memory bus and the buffers (DRAM));

a re-programmable non-volatile memory; (Fig. 2, flash memory array) ;

memory access logic operatively coupled to the memory bus and to the re-programmable non-volatile memory (Fig. 2 the flash controller serves as an interface between the memory bus and the flash memory array); and

processor logic operatively coupled to the memory access logic to transfer data with the dynamic memory via the memory bus and to transfer data with the re-programmable non-volatile memory (Fig. 1, (11), the CPU is connected to the entire subsystem (Fig. 2 (20) via the memory bus – col. 3, lines 26-65)),

the memory access logic configured to detect a write operation to the re-programmable non-volatile memory (Fig. 4, the flow chart begins by attempting a write operation to the main memory (EEPROM)),

the processor logic configured to respond to the memory access logic detecting the write operation and to:

identify a caching location in the area of memory wherein data to be written by the write operation can be cached (the system attempts to determine a location to store the data in the cache – Fig. 4. Also note the microprocessor is used to carry out functions of the memory module (Fig. 2, element 20) – col. 3, line 66 through col. 4, line 19); and

store the data in the area of memory identified by the caching location (Fig. 4, the data is stored in the cache identified by the address (see also Fig. 3)).

As for claim 32, Hasbun teaches the method of claim 31 wherein the step of determining a caching location comprises:

determining if the data can be stored in the dynamic memory (Fig. 4, system determines if the cache has remaining space available), and if not then:

identifying one or more memory locations in the dynamic memory (Fig. 4, memory locations are identified to clear out the cache); and

writing content in the one or more memory locations to the re-programmable non-volatile memory (Fig. 4, once the cache has been cleared to the buffer, the data stored at those memory locations will invariably be written to the flash) and

providing an address in the dynamic memory as the caching location in the area of memory (continuing with the flow diagram in Fig. 4, data can be

stored to the cache either by writing it to the appropriate addressed line, or writing it to an empty line).

As for claim 33, Hasbun teaches the method of claim 32 wherein the step of determining a caching location in the dynamic memory is limited to determining a caching location in a segment of the dynamic memory (Fig. 4, caching locations (i.e. the space where the data is cached prior to being sent to the EEPROM is determined and written on a line by line basis. A single line is a segment of the cache)).

As for claim 34, Hasbun teaches the method of claim 31 further including detecting a second write operation to the area in the re-programmable non-volatile memory and writing the data associated with the second write operation to the area of memory identified by the caching location instead of writing the data to the area in the re-programmable non-volatile memory (Fig. 4, the flow diagram will continue to detect multiple write attempts to the EEPROM, and will continue to cache them in the DRAM until it is determined that no more free space is available. Each subsequent write is written to a unique line in the cache).

As for claim 35, Hasbun teaches the method of claim 31 further including detecting a second write operation to a second area in the re-programmable non-volatile memory, determining if there is a caching area in the dynamic memory that is associated with the second area and if there is then writing data associated with the second write operation to the caching area associated with the second area (referring to Fig. 3, the cache (Fig. 2, element 23) can associate each line of the cache with any one of the four unique blocks of the EEPROM – col. 4, lines 45 through col. 5, line 4).

As for claim 36, Hasbun teaches the method of claim 31 wherein an address space of the re-programmable non-volatile memory is equal to or greater than an address space of the dynamic memory (the cache is only used to buffer data to the much larger main memory (EEPROM). Once the cache is full, the data is loaded to the main memory, therefore the main memory is larger than the cache).

As for claim 37, Hasbun teaches the method of claim 32 wherein the step of identifying one or more memory locations is based on the size of the data (Fig. 4, memory locations are identified to clear out the cache based on the size needed to make room for incoming cached data).

As for claim 40, Hasbun teaches the method of claim 31 wherein the re-programmable non-volatile memory is one of an EEPROM (electrically erasable programmable read-only memory) or a flash memory (as per the rejection of claim 31).

As for claim 41, Hasbun teaches the method of claim 31 further including obtaining an address range which defines the area of memory in the dynamic memory (col. 4, line 36 through col. 5, line 4, the line to be written to the cache associated with the EEPROM block number can be written to any addressed line of the cache. Additionally note that since the buffer is written line by line, the address of each line must be determined before it is written to the cache).

As for claim 42, Hasbun teaches the method of claim 31 further including detecting a read operation from the re-programmable non-volatile memory and reading the re-programmable non-volatile memory to effect the read operation (col. 6, lines 45-

63 – a read operation can be performed by directing a read command to the EEPROM in order to read in the data stored in any of the addressed blocks of the EEPROM).

As for claim 43, Hasbun teaches method of claim 31 further including detecting a read operation from the re-programmable non-volatile memory and reading one or more memory locations from the area of memory in the dynamic memory to effect the read operation (col. 6, lines 45-63 – a read operation can be performed by directing a read command to the cache in order to read in the data stored in the cache).

As for claim 45, Hasbun teaches the data processing unit of claim 44 wherein the memory access logic is further configured to:

determine if the data can be stored in the area of memory (Fig. 4, system determines if the cache has remaining space available); and

provide an address in the area of memory as the caching location in the area of memory (continuing with the flow diagram in Fig. 4, data can be stored to the cache either by writing it to the appropriate addressed line, or writing it to an empty line),

wherein if it is determined that the data cannot be stored in the area of memory, then:

identify one or more memory locations in the area of memory (Fig. 4, memory locations are identified to clear out the cache); and

write content in the one or more memory locations to the re-programmable non-volatile memory, wherein the one or more memory locations are available for caching a write operation (Fig. 4, once the

cache has been cleared to the buffer, the data stored at those memory locations will invariably be written to the flash).

Claims 46 and 47 are rejected based on the same rational as claims 36 and 40 respectively.

As for claim 48 Hasbun teaches the data processing unit of claim 44 wherein the dynamic memory is a random access memory (as per the rejection of claim 44).

Claims 49 and 50 are rejected based on the same rational as claims 42 and 43 respectively.

8. Claims 51-55 are rejected under 35 U.S.C. 102(b) as being anticipated by Tobita et al. (US PG Publication 2002/0051394 A1), hereinafter Tobita.

As for claim 51, Tobita teaches a memory access method comprising:

detecting a write operation to a re-programmable non-volatile memory (paragraph 0047, all lines – data is initially stored in a write buffer. Once the transfer from the host terminates, the data is written to the flash memory (i.e. non-volatile memory). The system must inherently detect a write operation before a write can be performed); and

if a destination address associated with the write operation is within a first range of addresses, then performing a fast write operation of data associated with the write operation to the re-programmable non-volatile memory (referring to Fig. 48, paragraph 0240, all lines – fast write operation is performed on both the higher and lower order bits of memory (Fig. 48, element 1014)).

As for claim 52, Tobita teaches the method of claim 51 wherein the first range of addresses spans the entire address space of the re-programmable non-volatile memory (the entire memory (Fig. 48, element 1014) is written via a fast write operation).

As for claim 53, Tobita teaches the method of claim 51 wherein if the destination address is not within the first range of addresses, then performing a slow write operation of the data to the re-programmable non-volatile memory (note in Fig. 48, elements 1239 and 1014 can be combined such that the memory can be a mix of slow write and fast write memory (see also paragraph 0240, all lines). In this instance, the memory unit would either perform fast or slow write operations depending if higher order or lower order bits were being addressed. Note combining these two types of memory still constitutes "a re-programmable non-volatile memory", even though the two types happen to be on separate chips (i.e. the memory itself does not necessarily need to be monolithic based on Examiner's broadest reasonable interruption of the claim consistent with the specification (MPEP § 2111)).

As for claim 54, Tobita teaches the method of claim 51 wherein the first range of addresses spans a range of addresses less than the address space of the re-programmable non-volatile memory (an alternative to the memory shown in Fig. 48 (1014) would be one as per discussed in the rejection of claim 53. In this case, the memory unit with fast write capability would span less than the total available memory addresses)

As for claim 55, Tobita teaches the method of claim 51 wherein the step of performing a fast write operation is performed if the destination address falls within any

of a plurality of ranges of addresses (any address of the memory (Fig. 48, (1014)) would execute a fast write operation).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasbun (US Patent 5,696,929) as applied to claim 32 above, and in further view of Agarwal et al. (US Patent 5,530,958) hereinafter Agarwal.

As for claims 38 and 39, though Hasbun teaches all of the elements of claim 32, he fails to teach the step of identifying one or more memory locations as based on contents of the data, including applying a hash function on the data to produce a hash result, wherein the one or more locations are determined based on the hash result.

Agarwal however teaches a cache memory system and method with multiple hashing functions and hash control storage, which includes identifying memory locations, based on a hashing function. Additionally, Agarwal's system utilizes a CAM in which cached data is addressed by content (rather than size), in order to improve the hit rate of the system by storing the indexes of blocks that are present in rehashed locations (col. 3, lines 20-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Hasbun to further include Agarwal's cache memory system into his own flash EEPROM memory. By doing so, Hasbun could benefit from Agarwal's teachings by exploiting the improved cache memory system which incorporates a low conflict miss rate of a d-way associative cache, while maintaining the critical access path of a direct-mapped cache. This modification would result in improved performance over a victim cache present in Hasbun's system, as taught by Agarwal (col. 2, lines 21-51).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

. Tanaka (US Patent 5,581,726) teaches a control system for controlling a cache storage unit by using a non-volatile memory.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER